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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Y. Ben Moshe et al.
Case: 3-1-1-2-1-2
Serial No.: 09/544,054
Filing Date: April 6, 2000
Group: 2189
Examiner: Christopher E. Lee

Title: Modular Switch With Dynamic Bus

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: Teresa M. Hanli Date: October 27, 2003

REPLY BRIEF

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Sir:

This Reply Brief is submitted in response to the Examiner's Answer dated August 26, 2003 in the above-referenced application.

ARGUMENT

The Examiner in his Answer to the Appeal Brief filed by Applicants on May 19, 2003, reasserts the argument that each of claims 1-11, 13-29 and 31-38 is unpatentable under 35 U.S.C. §102(b) or §103(a). Applicants respectfully disagree with the assertions presented by the Examiner in the Answer, for the reasons identified below, as well as for the reasons previously set forth in the Appeal Brief.

Applicants initially note that the Answer at page 2, item 7 states that "the rejection of claims 1-11, 13-29 and 31-38 stand or fall together . . . ." It is believed that this is an incorrect statement regarding the grouping of claims, in that it fails to conform to the requirements of 37 C.F.R. §1.192(c)(7). In the present application, there is no single "rejection" of claims 1-11, 13-29 and 31-

38. Instead, there are a total of sixteen different rejections applied to these claims, corresponding to Issues 1 through 16 as set forth in the Appeal Brief. Applicants stated as follows on page 4 of the Appeal Brief regarding grouping of claims:

> Certain of the above-enumerated Issues, namely, Issues 4, 5, 6, 8, 9, 10, 12, 14, 15 and 16, each involve only a single claim which stands or falls alone.
>
> For each of the remaining Issues, the multiple claims associated with that Issue stand or fall together.

It is believed that the foregoing statement from the Appeal Brief properly characterizes the grouping of claims. The statement made by the Examiner in the Answer at page 2, item 7 to the effect that "the rejection of claims 1-11, 13-29 and 31-38 stand or fall together" is incorrect, and should be withdrawn or otherwise corrected. Claims 1-11, 13-29 and 31-38 clearly do not stand or fall together.

With regard to the §102(b) rejections of independent claims 1, 13 and 23, the Examiner argues that these claims are anticipated by U.S. Patent No. 5,734,656 (hereinafter "Prince"), PCT Publication WO 93/15464 (hereinafter "Porter"), and U.S. Patent No. 5,771,358 (hereinafter "LaBerge"), respectively. Applicants respectfully submit that the Examiner has failed to establish anticipation of each of these independent claims by the corresponding reference.

Applicants note that §2131 of the Manual of Patent Examining Procedure (MPEP), Eight Edition, August 2001, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Independent claim 1 is directed to a modular switch. The modular switch as claimed comprises a plurality of backplane sub-buses, a plurality of cards which are each allocated one or

more of the backplane sub-buses, and a controller which dynamically allocates the backplane sub-buses to the plurality of cards, based on bandwidth needs of the cards.

The Examiner at page 3, section 10 of the Answer argues that the cell slots in FIG. 7 of Prince correspond to the plurality of backplane sub-buses of claim 1, and that LAN modules correspond to the claimed plurality of cards. The Examiner more particularly relies on the teachings in column 7, lines 33-37 of Prince, which provide as follows, with emphasis supplied:

> The switch fabric of the ATM switch, i.e., the ATM switch backplane bus, switches a cell based on routing information provided by the source LAN or ATM module to an output port on a destination LAN or ATM module of the switching hub.

There is no mention here or elsewhere in Prince regarding a plurality of backplane sub-buses as claimed. Moreover, Prince in fact teaches away from the claimed invention by teaching in conjunction with FIG. 4 and the associated text at column 11, lines 8-19, that a backplane bus 370 is separated into different physical portions 421 through 426, each of which is physically connected to each of the LAN modules 401 through 412. This is directly contrary to the claimed invention, which as noted above calls for dynamic allocation of backplane sub-buses to the plurality of cards, based on bandwidth needs of the cards.

The Examiner at page 15, section 11 of the Answer further argues that Applicants have somehow admitted that the term "sub-bus" as used in the present application can be interpreted to include a slot or set of slots of a time multiplexed bus. Applicants have made no such admission, and in fact argue exactly the contrary position at page 5 of the Appeal Brief, which provides as follows, the emphasis being in the original:

> The specification makes it clear that the term "sub-bus" as used therein refers to something other than a slot or set of slots of a time domain multiplexed bus.
>
> . . .
>
> The term "sub-bus" as used in the claims is therefore clearly distinct from a slot or set of slots of a time domain multiplexed bus, in accordance with the explicit teachings of

the specification. Applicants have in effect defined the term "sub-bus" in their specification to exclude a slot or set of slots of a time domain multiplexed bus.

Applicants thus argue that the term "sub-bus" as used in the specification cannot be interpreted as including a cell slot or other slot of a time domain multiplexed bus. In support of their argument, Applicants rely on the specification at page 1, lines 26-32, which states as follows, with emphasis supplied:

> In some switches, the bus is divided into sub-buses of the size of the maximal capacity of the cards. The sub-buses are allocated to the cards using time domain multiplexing. Such multiplexing, however, is wasteful as it gives all the cards the some [sic] amount of bandwidth regardless of their needs. In addition, this solution adds delay to packets received by a card when it is not its turn to use the bus. In some buses which use time domain multiplexing, the bus is divided into slots, and each time a transmitter needs to transmit data it requests an amount of slots. This solution, however, is too slow and complex for fast switches.

This portion of the specification makes it clear that sub-buses and slots are different things, as those terms are used in the present specification. In the first four sentences of the quoted passage, the term sub-bus is clearly used to refer to a physical portion of a given bus. The second sentence indicates that such physical sub-buses can be assigned to cards using time domain multiplexing. However, the use of time domain multiplexing to allocate physical sub-buses does not mean that the physical sub-buses comprise time slots *per se*. The physical sub-buses referred to at page 1, line 27 of the specification are in fact not time slots, but are instead physical portions of a given bus, in this case physical portions each having a size corresponding to the maximal card capacity.

Time slots are specifically referred to in the final two sentences of the quoted passage, and are thus clearly distinguished from sub-buses. The quoted passage refers to two entirely distinct prior art "solutions," namely a first solution involving separation of a bus into physical sub-buses, with allocation of the different physical sub-buses to the cards using time domain multiplexing, and

a second solution which does not separate a bus into physical sub-buses, but instead separates the bus into slots, and uses time domain multiplexing of the slots. In the second solution, there are no separately-identifiable physical sub-buses. The quoted passage from the specification indicates that the two solutions are entirely distinct, and exhibit different sets of problems.

Applicants therefore again submit that the quoted passage from the specification clearly identifies sub-buses as being distinct from time slots. In claim 1, Applicants chose to utilize the term sub-bus, and thus chose to exclude arrangements involving separation of a bus into time slots. Applicants are entitled to be their own lexicographers in this manner. In view of the decision by Applicants to distinguish sub-buses from time slots in their specification, and to utilize the former term in their claims, it is improper for the Examiner to attempt to assert that sub-buses read on time slots in formulating a rejection of claim 1.

As noted above, time slots such as the cell slots in FIG. 7 of Prince, that are relied upon by the Examiner as being allegedly anticipatory of the claimed sub-buses, are clearly distinguished from sub-buses in the explicit language of the specification. Applicants in claim 1 specifically recite "a plurality of sub-plane buses," and thus are not attempting to argue "features . . . not recited in the rejected claim(s)" as alleged by the Examiner on page 16, first paragraph of the Answer. Instead, Applicants are simply relying upon the specification to show what is meant by a claim term, and this is entirely appropriate.

The anticipation rejections of independent claim 13 over Porter, and claim 23 over LaBerge, are deficient for reasons similar to those described above.

Like Prince, Porter is directed to a single physical bus. Therefore, Porter does not disclose "a plurality of backplane sub-buses" or the related limitations as recited in independent claim 13, for reasons similar to those described above with reference to independent claim 1. The Examiner at page 8 of the Answer argues that the "plurality of backplane sub-buses" in claim 13 is disclosed by the N switched lines of FIG. 3 in Porter, and that the claimed "plurality of cards configurable to listen to a variable number of the backplane sub-buses" is disclosed by the teachings on page 1, lines 9-10, page 3, lines 21+, page 4, lines 2-9 and page 15, line 25 to page 16, line 2 of Porter. However, the N switched lines of FIG. 3 comprise the entire backplane bus which is N lines wide. In addition, if the "plurality of cards" as claimed correspond to the boards referred to in Porter, such boards are

not disclosed as being configurable in the manner claimed. Instead, Porter teaches to utilize a separate switch array between the backplane bus and the boards. This is clear from the following description taken from page 7, lines 1-5 of Porter, with emphasis supplied:

> The invention provides a backplane having a plurality of lines constituting a bus extending therealong, a plurality of slots connecting with said lines and providing connections with a similar plurality of boards, there being provided a condition-variable switch array between the lines and each slot.

The switch array in Porter is not part of any of the boards. The boards in Porter are therefore not configurable in the manner claimed.

The LaBerge reference similarly fails to meet the limitations of independent claim 23. This claim is directed to a method of allocating sub-buses to cards of a switch, and includes the steps of determining bandwidth needs of each of the cards, assigning each of the cards a bus demand value which is a function of the bandwidth needs of the card and the current bandwidth allocated to the card, and allocating the sub-buses to the cards based on the bus demand values of the cards. Like Prince and Porter, the LaBerge reference fails to disclose sub-buses as claimed. The arguments presented above with regard to independent claim 1 are therefore equally applicable to the anticipation rejection based on LaBerge.

The Examiner at page 11 of the Answer argues that the cards recited in claim 23 are disclosed by bus requesters 26, 28, 30 and 32 of FIG. 1 in LaBerge, and that the switch recited in claim 23 is disclosed by the bus controller 24 of FIG. 1 in LaBerge. However, if the bus controller 24 of LaBerge corresponds to the switch of claim 23, then it is clear that the bus requesters 26, 28, 30 and 32 are not "cards of a switch" as required by the claim. Instead, these bus requesters 26, 28, 30 and 32 are all external to the bus controller 24, and represent main memory, hard drive A, hard drive B and PCI bus elements, respectively, of a computer system. See LaBerge at column 2, lines 33-34 and 46-47. Standard computer system elements such as main memory, hard drives and a PCI bus cannot reasonably be construed as being anticipatory of "cards of a switch" as claimed. There is

certainly no teaching of suggestion in LaBerge to that effect. The arrangements of LaBerge are therefore clearly not anticipatory of all limitations of claim 23.

The Examiner further argues at page 16 of the Answer that Applicants in asserting the foregoing argument are relying upon "features . . . not recited in the rejected claim(s)." Applicants respectfully disagree. Claim 23 specifically refers to allocation of sub-buses to cards of a switch. Thus, there are a plurality of sub-buses at issue in the claim. As indicated above in the context of claim 1, the term "sub-bus" as described in the specification refers to a portion of a physical bus, and not to a time slot or set of time slots. Applicants are again simply relying upon the specification to show what is meant by the claim term "sub-bus," and this reliance on the specification is entirely appropriate.

With regard to the §103(a) rejection of independent claim 31, this claim is directed to a modular switch comprising a plurality of communication cards, a plurality of backplane sub-buses which are used for communication between groups of the cards, and at least one controller. The controller is configurable to divide the cards into different numbers of groups, such that the cards of the different groups do not transmit data to each other, and is further configurable to allocate the sub-buses to the cards based on bus demand values of the cards. The Examiner argues that this claim is obvious in view of a proposed combination of Porter with LaBerge. Applicants disagree. Porter is directed to a computer backplane having line switches, while LaBerge is directed to a processor bus shared by a plurality of processors in a computer system. The deficiencies of these references as applied individually to respective claims 13 and 23 were outlined above. Collectively, the references simply fail to disclose an arrangement in which backplane sub-buses of a modular switch are allocated to communication cards of the modular switch based on bus demand values of the cards.

As Applicants noted in their Appeal Brief, the Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). The Federal Circuit has further stated that "conclusory statements" by an examiner fail to adequately

address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344.

Applicants submit that the Examiner has failed to provide any objective evidence of motivation to modify the teachings of Porter and LaBerge to meet the particular limitations of independent claim 31. Instead, the Examiner provides the following statement of obviousness at page 12 of the Answer, with emphasis supplied:

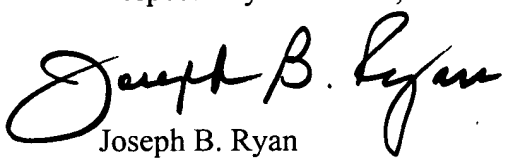
> Therefore, it would have been obvious [to] one of ordinary skill in the art at the time the invention was made to have applied said bandwidth allocation method, as disclosed by LaBerge, to said modular switch, as disclosed by Porter, for the advantage of apportioning said bandwidth based on said bus demand value enables higher bandwidth cards to continue to operate at a relatively high bandwidth when said bus is saturated (See LaBerge, col. 6, lines 19-21).

This appears to be a conclusory statement of obviousness based on the type of "subjective belief and unknown authority" that the Federal Circuit has indicated as being insufficient to support an obviousness rejection. The "bus requesters" referred to in the cited portion of LaBerge at column 6, lines 19-21, as indicated previously herein, comprise main memory, hard drive and PCI bus elements of a computer system. Therefore, one skilled in the art would not be motivated to look to teachings regarding the LaBerge bus requesters for application in the backplane of Porter. It therefore appears that the Examiner has simply attempted a hindsight-based reconstruction of the invention as set forth in claim 31.

Moreover, one would expect, based on the teachings in Porter regarding FIG. 1 thereof, that such generic computer system elements would be associated with processing unit(s) 11, and would be connected thereto directly rather than through the backplane 10. This is because such generic computer system elements do not have process-specific functions, and thus would generally be shared by each of the process stages 13, 14 and 15. See Porter at page 4, last four lines, to page 5, line 8. Porter thus teaches away from the proposed combination with LaBerge.

For the reasons identified above and in the previously-filed Appeal Brief, Applicants respectfully submit that the §102(b) and §103(a) rejections are improper and should be withdrawn.

Respectfully submitted,



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